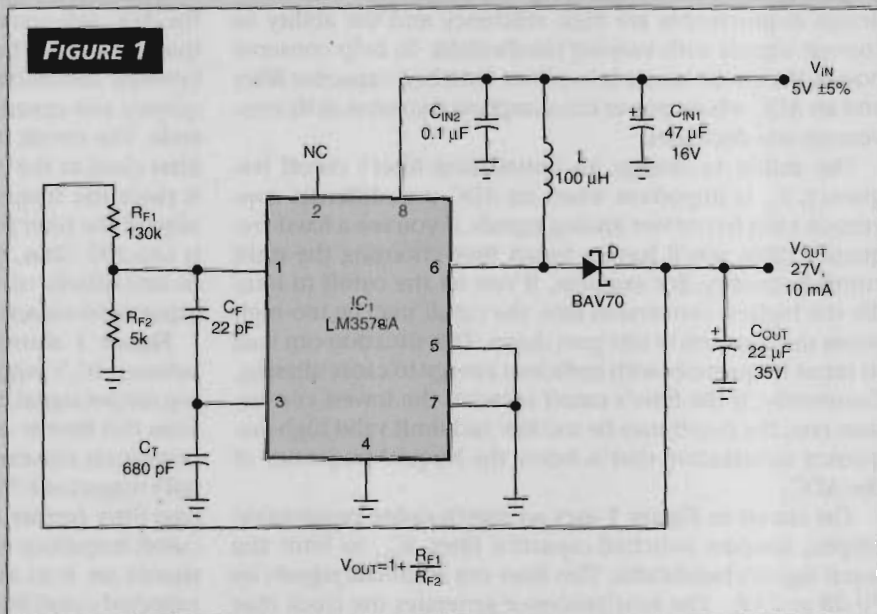


Low-cost circuit biases VCOs for cable and TV

RAVINDRA AMBATIPUDI, NATIONAL SEMICONDUCTOR CORP, SANTA CLARA, CA

PLLs are useful in a variety of applications, most notably cable and TV tuners. In these systems, the PLL synchronizes an output signal (typically from a VCO) with a reference or input signal, in frequency as well as in phase. The VCO in these PLLs requires a biasing circuit. Depending on the VCO, this biasing circuit must provide an output voltage of 24 to 32V from an input voltage of typically 5, 9, or 12V. A low-cost VCO-biasing circuit converts a 5V input to a 27V bias-level output (Figure 1).

Timing capacitor C_T sets the switching frequency. A value of 680 pF sets the switching frequency to 100 kHz. Capacitor C_F (typically 10 to 25 pF), together with feedback resistors R_{F1} and R_{F2} , provides compensation. You can find more details on the choice of these components in the LM3578A data sheet. With a slight modification, the same circuit works with a 9 or 12V input. The circuit simply requires a higher voltage input capacitor and a higher value inductor. Because the current requirements are so low, you can use inexpensive inductors and capacitors. Capacitor C_{IN2} suppresses the switching noise; you can use an inexpensive filter to further suppress the noise. The noise is a function of the ESR of the input and

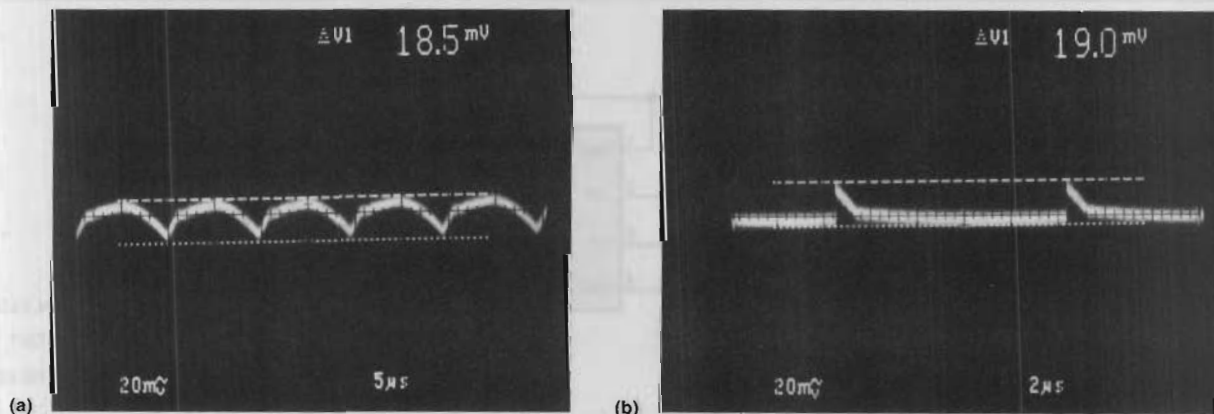


An inexpensive circuit provides VCO bias for cable and TV-tuner applications.

output capacitors (Figure 2a and b). The circuit in Figure 1 is easy to implement using a 2-to-1-scale pc-board layout. (DI #2110)

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FIGURE 2



The input (a) and output (b) ripple for Figure 1's VCO-biasing circuit are 18.5 and 19 mV p-p, respectively.

Filter cutoff tracks ADC conversion rate

KEVIN R HOSKINS, LINEAR TECHNOLOGY CORP, MILPITAS, CA

The circuit in **Figure 1** matches an antialiasing filter's cutoff frequency to an ADC's changing conversion rate. Two main design requirements are high efficiency and the ability to convert signals with varying bandwidths. To help conserve power, the circuit uses a low-power switched-capacitor filter and an ADC whose power consumption decreases as its conversion rate decreases.

The ability to change an antialiasing filter's cutoff frequency, F_c , is important when an ADC uses different conversion rates to convert analog signals. If you use a fixed-frequency filter, you'll have a tough time choosing the right cutoff frequency. For example, if you set the cutoff to handle the highest conversion rate, the cutoff may be too high when the conversion rate goes down. This situation can lead to input frequencies with sufficient energy to cause aliasing. Conversely, if the filter's cutoff matches the lowest conversion rate, the cutoff may be too low and limit valid high-frequency information that is below the Nyquist frequency of the ADC.

The circuit in **Figure 1** uses an eighth-order, progressive, elliptic, lowpass switched-capacitor filter, IC₁, to limit the input signal's bandwidth. This filter can attenuate signals by 70 dB at $2 \times F_c$. The host processor generates the clock that controls the filter's cutoff frequency. IC₃ derives the conversion clock for the ADC, IC₂, by dividing the filter's clock by 2. For this design, the master clock is 400 kHz, so the ADC clock is 200 kHz.

The host processor requests a conversion by asserting a logic low on the CHIP SELECT line, which connects to the CS/SHDN input pin of the ADC. When CS/SHDN is a logic low, the ADC takes 15 clock cycles to generate conversion data. The host processor must assert a logic high on the CS/SHDN pin for at least 2 μ sec before the start of the next conversion.

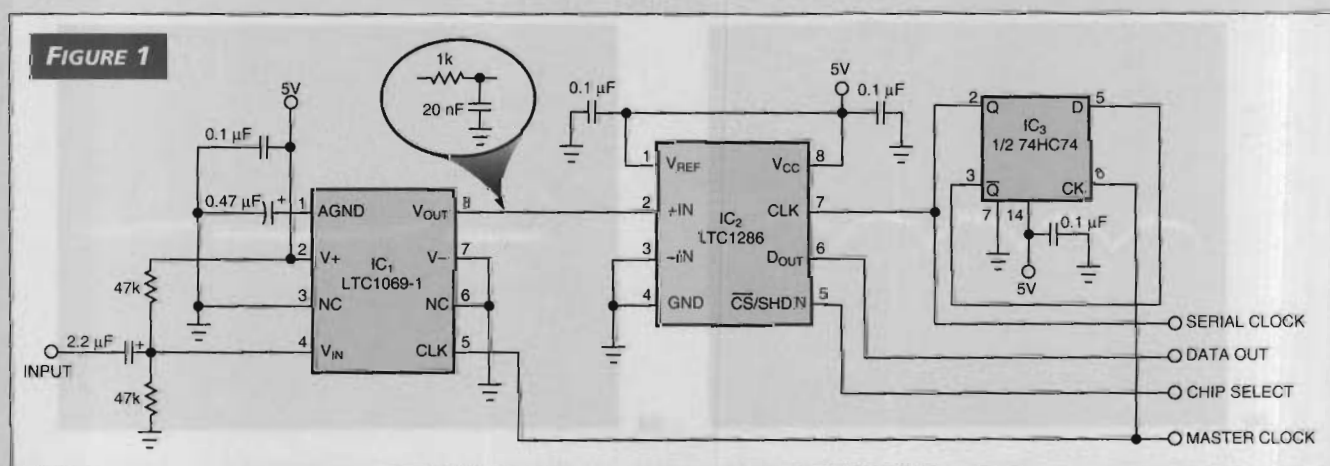
The maximum serial-clock frequency of 200 kHz for the

ADC sets the maximum conversion rate at 12.5k samples/sec. With this conversion rate, the maximum input signal that the ADC can convert without causing aliasing errors is less than 6.25 kHz. The filter's cutoff frequency is a compromise between maximum attenuation at twice the sampling frequency and ensuring that the filter's passband is sufficiently wide. The circuit achieves this compromise by running the filter clock at the master-clock frequency of 400 kHz, which is twice the frequency of the ADC's conversion clock. The ratio of the filter's cutoff frequency to its CLK input at Pin 5 is 1-to-100. Thus, $F_c = 400 \text{ kHz} / 100 = 4 \text{ kHz}$, which is also equal to one-fiftieth of the ADC's conversion clock. The filter's input network sets a highpass cutoff of 3.1 Hz.

Figure 1 shows an optional passive-RC lowpass filter between IC₁'s output and the ADC's input. Relative to a 2V p-p output signal, the magnitude of any residual clock signal from this filter is -80 dB. However, the residual clock signal's magnitude remains constant, independent of the output signal's magnitude. Therefore, using the simple passive-RC lowpass filter further attenuates clock-signal feedthrough. The cutoff frequency of this passive filter is not critical, but you should set it to at least one octave above IC₁'s maximum expected cutoff frequency. The values in **Figure 1** set the cutoff frequency for the passive lowpass network at 8 kHz.

One area that requires attention is filter settling time. When a filter's cutoff frequency changes, a minimum amount of time has to elapse before the output settles to within a given error band. IC₁'s eighth-order elliptic filter requires $13.5/F_C$ to settle within a 12-bit-resolution error band, so the filter requires 13.5/4 kHz, or 3.4 msec, to settle. Once the filter settles, the ADC can begin generating conversions. At a cutoff frequency of 100 Hz, the filter's settling time is 135 msec. (DI #2115)

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**FIGURE 1**

Clocking the switched-capacitor filter with an integer multiple of the ADC's serial-clock frequency—in this case 2×—allows the filter's cutoff frequency to track the ADC's sampling rate.

Pulse discriminator excises narrow pulses

MARK VITUNIC, MICRO LINEAR, SAN JOSE, CA

The circuit in Figure 1 deletes narrow pulses from fixed-frequency PWM waveforms. The output of the circuit effectively represents a delayed version of the input with both low and high narrow pulses deleted. Unlike using a lowpass filter to remove narrow pulses, this circuit preserves the width of pulses wider than the circuit's RC time constants.

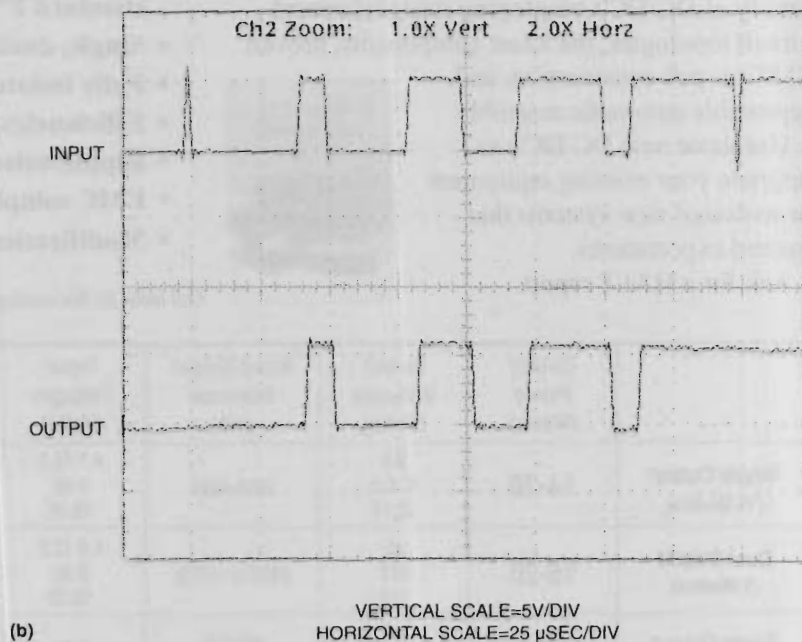
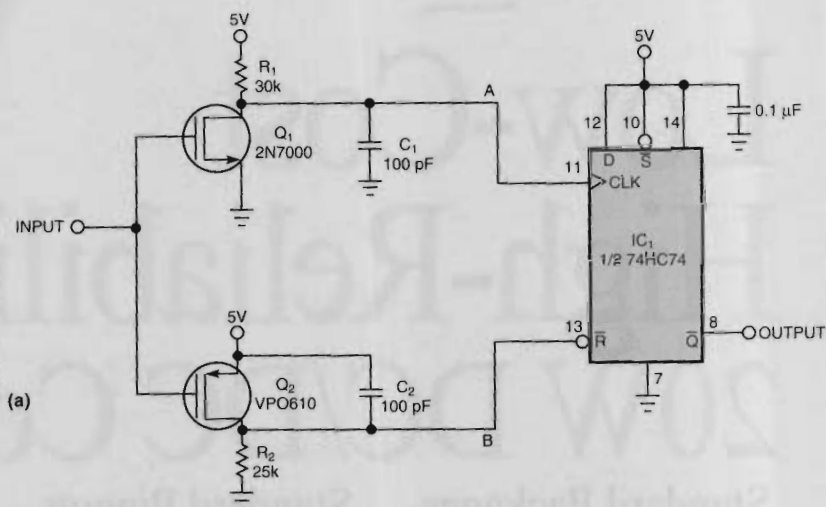
A pulse discriminator is useful for a PWM signal that serves as an input to a power inverter that in turn drives an electric motor. Deleting narrow pulses results in reduced inverter switching losses with no perceivable difference in motor response due to the high motor time constant. This circuit also eliminates the potential of a narrow pulse discharging the bootstrap capacitor in a high-side driver.

Q_1 , R_1 , and C_1 implement an inverting delay circuit, which produces a signal at node A that has fast high-to-low transitions and slow low-to-high transitions. Node A is the clock input to a D flip-flop, IC₁. Q_2 , R_2 , and C_2 implement a second inverting delay circuit that produces fast low-to-high transitions and slow high-to-low transitions at node B. Node B is the flip-flop's reset input.

If the input pulse width, low or high, is shorter than $0.693 \times R_1 \times C_1$ or $0.693 \times R_2 \times C_2$, respectively, the delayed pulses at nodes A and B do not trip the CMOS-logic thresholds at the input of IC₁. The values of R_1 and R_2 differ slightly because the CMOS-logic threshold of IC₁ is not perfectly symmetrical with respect to V_{DD} .

With the values of the RC time constants in Figure 1a, the circuit deletes pulses approximately equal to 3 μ sec or less. Input and output waveforms of the circuit using a 25-kHz PWM input with pulse widths of 2.5, 10, 20, 30, and 37.5 μ sec show the removal of the 2.5- μ sec pulses (Figure 1b). To improve the pulse-width control, you can replace R_1 and R_2 with fixed-value current sources. (DI #2118)

FIGURE 1



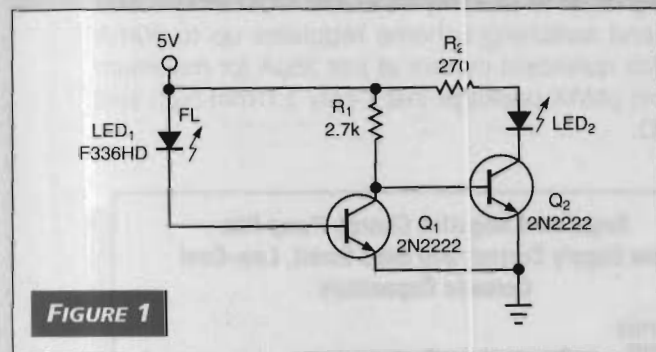
Two delay paths prevent narrow pulses from tripping the logic thresholds of a D flip-flop (a). The resultant PWM output waveform shows the selective deletion of narrow pulses, in this case, pulses narrower than 3 μ sec (b).

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Alternating LED flasher uses minimal parts

DENNIS EICHENBERG, PARMA HEIGHTS, OH

A pair of alternating flashing LEDs makes an excellent visual alarm. One of the LEDs remains illuminated, so there's little chance the alarm will go undetected even by a casual glance. Several circuits can provide this function, but the one



Two alternately flashing LEDs in a low-parts-count configuration provide a noticeable visual alarm.

in Figure 1 is the simplest. The circuit is also reliable, compact, efficient, and inexpensive. The heart of the circuit is LED₁, an F336HD T-1 $\frac{3}{4}$ red flashing LED (part number 276-036 at Radio Shack). It operates directly from 5V and provides a consistent light pulse at approximately 1 Hz without a time-constant capacitor.

The F336HD starts immediately when you apply power, and it's insensitive to temperature variations. LED₂ is a standard T-1 $\frac{3}{4}$ red LED (part number 276-041 at Radio Shack). The on-state current pulse through LED₁ is approximately 10 mA; it is 0 mA in the off state. This current flows through the base of Q₁ to turn it on. Resistor R₁ biases Q₂ on until Q₁ turns on. When Q₁ turns on, Q₂ and LED₂ turn off. When LED₁ turns off, Q₁ turns off, Q₂ turns on, and LED₂ turns on. Resistor R₂ provides current limiting for LED₂; R₂'s value produces brightness in LED₂ approximately equal to that of LED₁. (DI #2106)

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Shunt battery charger provides 1A continuous current

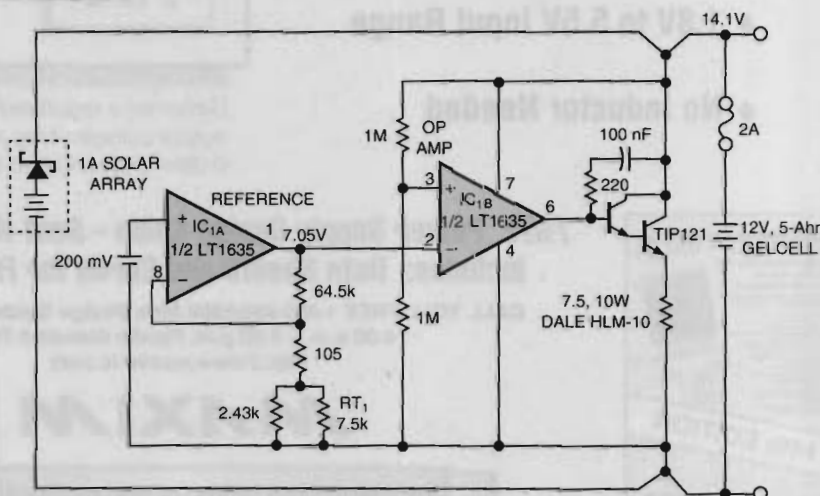
MITCHELL LEE, LINEAR TECHNOLOGY CORP, MILPITAS, CA

Most battery chargers use nothing more than a series-pass regulator with current limiting. In solar-powered systems, you can't count on having sufficient head room to keep a series regulator alive, so a shunt method is preferable. An example of a simple shunt battery charger consists of an op amp driving a shunt transistor and ballast resistor (Figure 1). The heart of the circuit is IC₁, an LT1635, which contains an op amp and a reference. Operation is straightforward. A feedback divider comprising two 1-M Ω resistors senses the battery voltage. The circuit amplifies the internal 200-mV reference to 7.05V and compares this voltage with the feedback signal.

Temperature sensor RT₁ introduces a temperature coefficient that accurately tracks the battery's correct charging voltage over a wide temperature range. Because RT₁ compensates for changes in battery temperature, position it close to the battery and as far as possible from the shunt elements. When the battery charges to 14.1V, the op amp's output voltage begins to rise, turning on the Darlington shunt and resisting further changes in voltage. Full panel power

divides equally between the transistor and the 7.5 Ω resistor when the battery is completely charged. Provide adequate heat sinking and airflow for dissipation as high as 15W.

FIGURE 1



NOTE: RT₁=THERM-O-DISC (MANSFIELD, OH) 1K752J.

This temperature-compensated shunt battery works with solar panels in applications providing insufficient head room for a series-pass charger.

The charger can handle 1A continuous current, which is compatible with a 20W panel. It's unnecessary to disconnect or diode-isolate the charger during periods of darkness, because the standby current is only 230 μ A—less than 10% of the self-discharge current of even a small battery. If you need a different or an adjustable output, you can easily modify the feedback ratio at the 1-M Ω divider. A good compromise between an aggressive charge voltage and a conservative float voltage is 14.1V. Given the cyclic nature of insolation, periodic charging at 14.1V is not detrimental

to Gelcells (Johnson Controls Inc, Milwaukee).

The circuit in **Figure 1** works with larger or smaller batteries than the one shown. As a rule of thumb, you should size the panel from 1W per 10-Ahr battery capacity (a float charge under good conditions with a good battery) to 5W per 1-Ahr battery capacity (a one-day recharge of a completely discharged battery under favorable conditions of insolation). (DI #2114)

EDN

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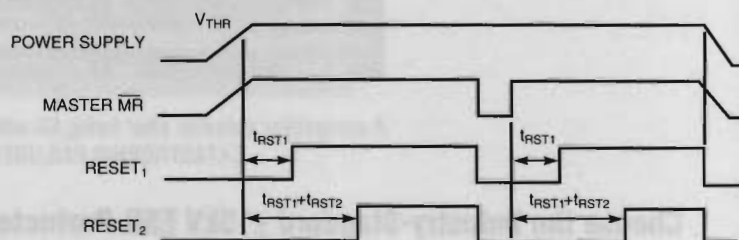
Reset ICs create sequenced or long resets

DOUG ANDERSON, ELECTRONIC TECHNOLOGY CORP, AMES, IA

Reset-generator ICs offer an inexpensive way to generate reliable reset signals for μ C and μ P applications. Certain applications, such as multiple-processor systems, require multiple resets that occur in a predictable sequence. You can use multiple-reset generators together to address the needs of these applications (**Figure 1**). The Reset output of IC₂ connects to the MR input of IC₂. In this configuration, the reset time-out period of IC₂ does not begin until the reset time-out period of IC₁ is complete, thus creating sequenced resets. Also, the Reset output of IC₂ now has a time-out period that is twice as long as that of a single reset generator.

You can similarly connect additional reset generators in sequence to create additional sequenced reset signals or even longer reset time-out periods. The first reset generator in the sequence is the master. You select it to have a higher reset threshold (4.63V for the ETC811L) than those of the slave reset generators (4.38V for the ETC811M). As the supply voltage increases during

FIGURE 2

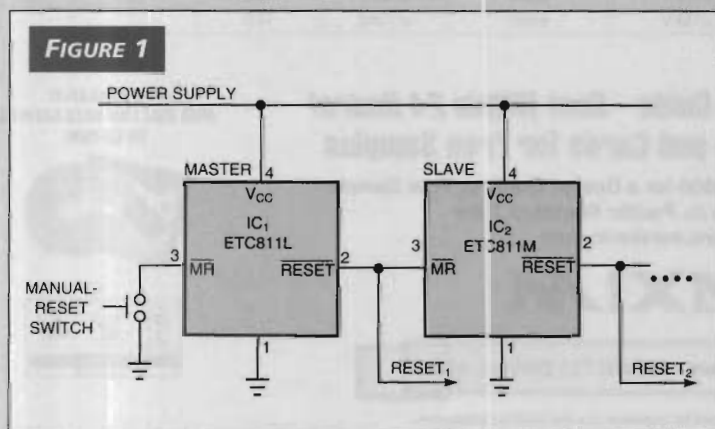


The circuit of **Figure 1** uses a master-slave configuration. Upon power-up, the master forces all the slaves to remain reset until the voltage reaches the master's reset threshold.

power-up, it reaches the reset threshold of the slave devices first (**Figure 2**). At this point, however, the supply voltage does not exceed the reset voltage of the master. Thus, the master holds Reset low and forces all the slaves to remain reset.

As the supply voltage increases further, it exceeds the threshold of the master, and the sequence of resets begins. In a similar fashion, as the voltage decreases during power-down, it first reaches the master's reset threshold. The master brings its Reset low, forcing all the slaves' Reset pins low in rapid succession. If the application requires a manual reset, you can attach a pushbutton switch to the MR pin on the master. The MR pin has an internal pullup to V_{CC} . When the switch closes, the Reset pins go high in the same sequence as upon power-up. Reset generators are available with other reset thresholds (3.08V for the ETC811Y, 2.93V for the ETC811S, and 2.63V for the ETC811R), so you can use this technique in 3V systems as well. (DI #2112)

EDN



Reset-generator ICs with differing reset thresholds allow you to configure sequenced or extra-long resets.

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Circuit takes square root of input voltage

MARK SHILL, BURR-BROWN CORP, TUCSON, AZ

For an NMOS transistor operating in the saturation region, the relationship between the drain current, I_D , and the gate-source voltage, V_{GS} , is governed by the square-law equation

$$I_D = \frac{\mu_N C_{OX} W}{2L} (V_{GS} - V_T)^2 = k(V_{GS} - V_T)^2, \quad (1)$$

where V_T is the threshold voltage and μ_N , C_{OX} , L , and k are constants not relevant to the square-law relationship.

You can algebraically manipulate Equation 1 to yield the gate-source voltage as a function of the drain current:

$$V_{GS} = \sqrt{\frac{I_D}{k}} + V_T, \quad (2)$$

where I_D is the drain current.

By using the transfer function of Equation 2, you can make a circuit take the square root of an input voltage. Such an implementation uses an NMOS transistor to obtain the square root of a positive input voltage, V_{IN} (Figure 1). The op-amp gain stage using IC_1 inverts V_{IN} ; the inversion is necessary because of the polarity of the I_D flow in MOSFET Q_1 . If you configure op amp IC_1 for a gain of -1, the drain current of Q_1 becomes $I_D = V_{IN}/R_3$.

Q_1 is an SD215 enhancement-mode n-channel MOSFET from Siliconix (Santa Clara, CA). It connects in the feedback loop of op amp IC_2 such that IC_2 's output voltage biases Q_1 's gate in relation to drain current I_D . The body terminal of Q_1 connects to the source terminal to eliminate any back-body voltage effects. Diode D_1 provides feedback and clamps the output of IC_2 when $V_{IN} \leq 0V$ and Q_1 turns off. Because the inverting terminal of IC_2 is at a virtual-ground potential, the output voltage of IC_2 is in effect the gate-source voltage, V_{GS} , of Q_1 . Thus, substituting $I_D = V_{IN}/R_3$ into Equation 2, the output voltage of IC_2 assumes the relationship

$$V_{GS} = \sqrt{\frac{V_{IN}}{R_3 \cdot k}} + V_T = \sqrt{\frac{1}{R_3 \cdot k}} \sqrt{V_{IN}} + V_T. \quad (3)$$

To eliminate the first radical term and V_T from Equation 3, the output voltage of IC_2 connects to an INA118 instrumentation amplifier. The negative-input terminal of the INA connects to a bias level of approximately 1V, approximating the MOSFET's threshold voltage, V_T . The gain of the INA is $\sqrt{R_3 \cdot k}$, or approximately 6 V/V. The gain of the INA118 is $1 + 50k/R_G$, where R_G is an external gain-setting resistor. A 20-k Ω , 20-turn potentiometer provides both sufficient range and resolution.

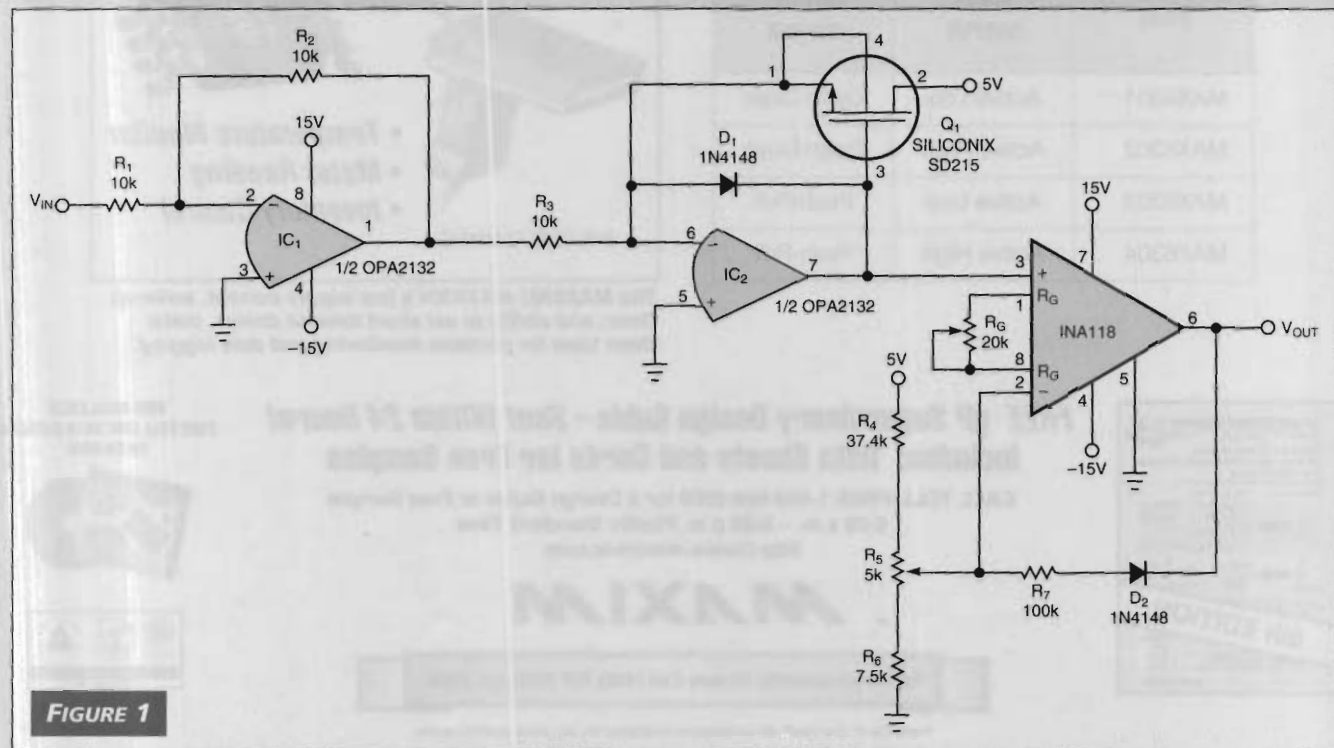


FIGURE 1

A circuit that extracts square roots uses the square-law relationship between a MOSFET's gate-source voltage and drain current.

To calibrate the square-root circuit, first vary V_{IN} between two accurate voltage levels, such as 9 and 1V. Then monitor V_{OUT} and adjust the gain-setting resistor, R_G , until the corresponding peak-to-peak output voltage, $V_{OUT'}$, is equal to $\sqrt{9V} - \sqrt{1V} = 2V$. Finally, adjust the offset voltage using potentiometer R_5 such that $V_{OUT} = 1V$ for $V_{IN} = 1V$. Transistor Q_1 begins to operate in the subthreshold region for input voltages lower than approximately 1V and thus no longer follows the square-law equation. Therefore, V_{OUT} can drop off quickly and even become negative for low input-voltage levels.

Once the voltage output of IC_2 approaches the threshold voltage set by R_5 , the output voltage of the INA118 approaches 0V. As the output of IC_2 becomes less than the threshold voltage, V_T , for low Q_1 drain current, the INA's output becomes negative. The addition of diode D_2 and resistor R_7 improves low-voltage performance. As Q_1 enters the subthreshold region and the INA's output pulls toward 0V, diode D_2 forward-biases and lowers the threshold voltage set at the INA's negative input. This addition improves the square-root transfer function for input voltages of 0.5 to approximately 1V.

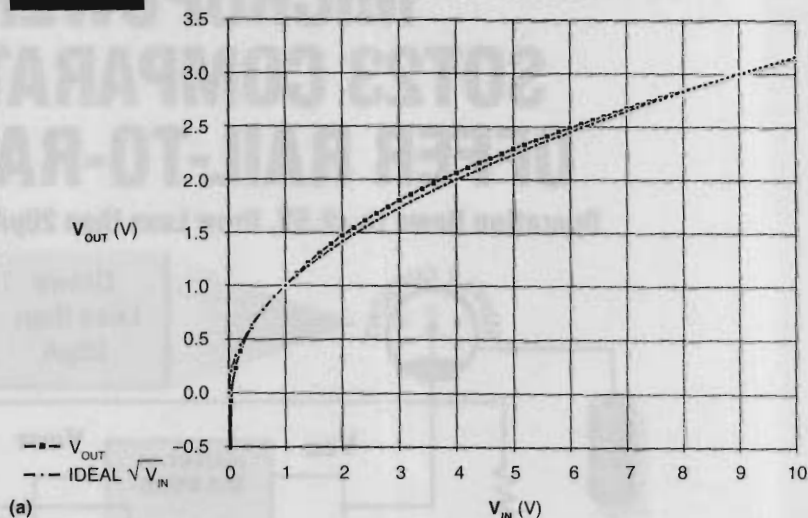
For input voltages of 0.5V to 10V, the maximum error is 70 mV (Figure 2). If you use a reduced input-voltage range, you can further improve the square-root accuracy by calibrating over the reduced-range endpoints. To prevent the output response from going below 0V for input voltages lower than 0.5V, connect the optional clamping circuit in Figure 3 to the INA118's output. (DI #2111)

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A simple addition to the circuit of Figure 1 prevents the instrumentation amplifier's output from going negative for low input voltages.

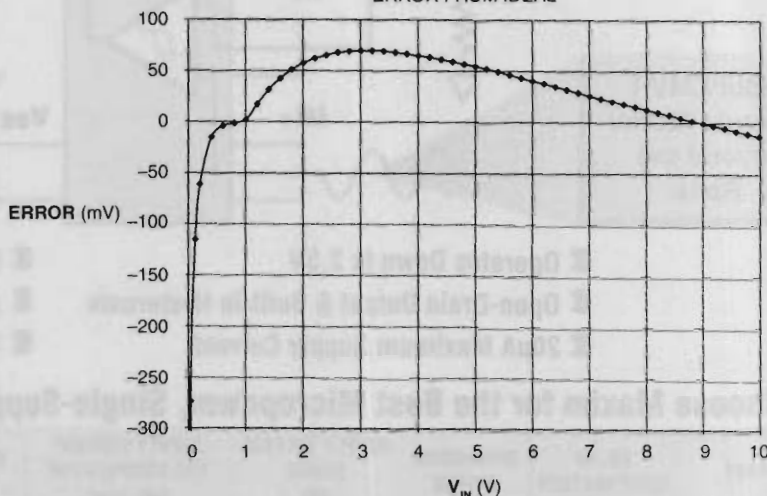
FIGURE 2

OUTPUT VOLTAGE OF SQUARE-ROOT CIRCUIT



(a)

ERROR FROM IDEAL



(b)

The transfer function for the circuit in Figure 1 follows an almost-ideal curve (a); the error is less than 70 mV over most of the circuit's useful range (b).

FIGURE 3

